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Comparative Study of I_{on}/I_{off} Ratio of Silicon Nanowire Transistor (SNWT) with Planner MOSFET

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Abstract

In this paper, a general approach, that considers both electrostatic integrity and quantum confinement, so called the "EQ approach", to compare the device performance of nanoscale Si FETs with various gate geometry configurations, i.e., planar MOSFETs versus SNWTs, is proposed. A better gate control, e.g., a better sub threshold swing and a higher ON-OFF current ratio is reported. This approach is based on the use of $L_Q$vs. $L_E$plot, where L_Q is the quantum confinement length, and L_E denotes the electrostatic scale length.

Keywords: Si-nanowire, Quantum confinement, Electrostatic scale length, SNWT, MOSFET.

1. INTRODUCTION

The electrostatic scale length (L_E) describes the significance of the 2D (in planar FETs) or 3D (in non-planar FETs) effects such as Drain Induced Barrier Lowering (DIBL) and V_T (threshold voltage) roll off in the device [1]. To be specific the larger the ratio L_E / $L_{Channel}$, the more serious would be the 2D/3D effects. The quantum confinement length (L_Q) is defined as [2]:

$$L_Q = \left| {k_B T} \Big/ {(dE_0/dT_{Si})} \right| \qquad (1)$$

Where,$E_0$is the lowest electron sub band level in the quantum mechanically confined Si body, T_{Si} is the Si body thickness, k_B is Boltzmann constant and T is the ambient temperature. While computing

the L_Q of a SNWT, the Si body width (W_{Si}) is assumed to be proportional to T_{Si}. Thus, changing T_{Si} does not alter the shape of the cross-section but only its area [3].

If the silicon body thickness variation in a FET is $\Delta T_{Si,}$ then the threshold voltage variation, ΔV_T can be obtained approximately as:

$$\Delta V_T \cong \left|\frac{\Delta E_0}{q}\right| = \left|\frac{dE_0}{dT_{Si}}\frac{\Delta T_{Si}}{q}\right| = \frac{k_B T \,.\, \Delta T_{Si}}{q\left|\frac{k_B T}{\frac{dE_0}{dT_{Si}}}\right|} = \frac{\Delta T_{Si}}{L_Q}\frac{k_B T}{q} \qquad (2)$$

Where, q is the charge of an electron. It is apparent from equation (2) that, the larger the L_Q the smaller the threshold voltage variation. So, L_Q explicitly represents the sensitivity of threshold voltage variation to Si body thickness fluctuation. Based on the definitions of L_Q and L_E, it is easily concluded that a well-temperature device structure should have a large L_Q (e.g., $L_Q > \Delta T_{Si}$) as well as a small L_E (e.g., $L_E < L_{Channel}$). As a result, when plotting the L_Q vs. L_E curves for different device structures on the same figure, the one that has the largest L_Q at the same L_E offers the best device characteristics (considering both electrostatics and quantum confinement).

2. DEVICE STRUCTURE

The investigation of three types of device structure which is presented in this paper are: (I) the symmetric planar double gate (DG) MOSFET, which is the optimum planar structure in terms of gate control,(II) the gate-all-around cylindrical wire (CW) FET which provides the best electrostatic integrity among SNWTs [4], and (III) the rectangular wire (RW) FET. The device structures are shown in Fig 1. Two wafer orientation, (001) and (011) is considered in the simulation. For the (001) wafer, the z direction (shown in Fig 1) is in [001], while for the (011) wafer the z direction is in [011]. In CW FETs the W_{Si} / T_{Si} ratio is always equal to 1.

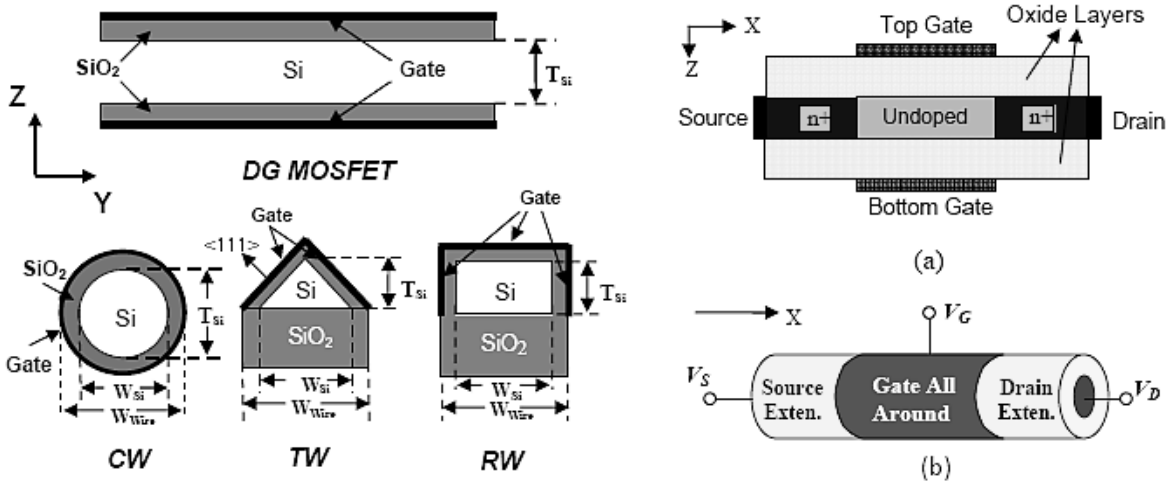

Figure 1: The cross-sections of the symmetric planar double-gate (DG) MOSFET and various nanowire FET structures – the cylindrical wire (CW), triangular wire (TW) and rectangular wire (RW) FETs. (The channel (x) direction is perpendicular to the paper surface.) Here T_{Si} is the silicon body thickness, W_{Si} is the silicon body width and W_{Wire} is the wire width. For the CW FET, $T_{Si} = W_{Si}$ is equal to the diameter of the circular Si body.

3. EQUATIONS FOR L_E AND L_Q:

3.1 Equations for the Electrostatic Scale Length L_E:

The electrostatic scale length L_E is a widely used parameter to describe the electrostatic coupling between the drain bias and the potential inside the channel, i.e., the larger the L_E, the stronger the coupling [5]. For a symmetric DG MOSFET, as indicated in [6] the L_E satisfies the equation:

$$\frac{\varepsilon_{Si}}{\varepsilon_{ox}} \tan\left(\pi T_{ox}/L_E\right) \tan\left(\pi T_{Si}/2L_E\right) = 1 \qquad (3)$$

Where T_{ox} is the oxide thickness, ε_{Si} and ε_{ox} are the dielectric constant for Si and SiO_2, respectively. By numerically solving Equation (3), L_E is computed for given T_{Si} and T_{ox}. For a cylindrical wire (CW) FET, following the same procedure, we obtained that L_E satisfies the following equation:

$$\varepsilon_{Si} \frac{J_0(-\pi T_{ox}/L_E + \chi_{01})}{J_1(-\pi T_{ox}/L_E + \chi_{01})} - \varepsilon_{ox} \frac{J_0(\pi T_{Si}/2L_E)}{J_1(\pi T_{Si}/2L_E)} = 0 \qquad (4)$$

Where, $J_o(x)$ and $J_1(x)$ are Bessel's function and value of $\chi_{01} = 2.4048$.

In general, to obtain L_E for a SNWT with arbitrary cross-section, a numerical solution of the 3D Laplace's equation:

$$\nabla\big(\varepsilon(y,z)\nabla V(x,y.z)\big) = 0 \qquad (5)$$

Here, V (x,y,z) is the electrostatic potential and ε (y,z) denotes the dielectric coefficient in the structure.

The solution of Equation (5) is decomposed into two domains: one in the x direction of the channel and other at the cross-section of the wire, i.e., $V_{(x,y,z)} = X_{(x)}.\ u_{(y,z)}$. Thus, two separate equations are obtained as:

$$\frac{\partial^2 X(x)}{\partial x^2} = K_n^2 X(x) \qquad (6)$$

and

$$-\nabla_{yz}\left(\varepsilon(y,z)\nabla_{yz}u(y,z)\right) = k_n^2 \varepsilon(y,z).u(y,z) \qquad (7)$$

Where, k_n are coefficients to be determined by satisfying the boundary conditions. The electrostatic scale length, L_E, is defined as $k_1 = \pi/L_E$, here, k_n^2can be viewed as the lowest Eigen value of Equation (7). To evaluate k_1, we discretize Equation (7) by the finite element method (FEM) subject to the boundary conditions, u(y, z) = 0 at the gate contacts.

3.2 Equations for the Quantum Confinement Length L_Q:

To evaluate the quantum confinement length L_Q of a device, we first need to obtain an expression for the lowest electron sub band level E_0. To do this, an ellipsoidal parabolic energy band for electrons is assumed and the effective-mass approximation [7] is adopted in this work. For simplicity, we neglect the penetration of electron wave function into the oxide layers (i.e., the electron wave function is zero at the Si/SiO_2 interface). It is also assumed that the potential profile variations in the cross-section are negligible, which is appropriate for ultrathin- body structures as confirmed by self-consistent Schrödinger-Poisson simulations. With these assumptions, an analytical expression can be obtained for a planar double gate (DG) MOSFET as:

$$E_0 = \frac{\hbar^2 \pi^2}{2 m_z^* T_{Si}^2} \qquad (8)$$

Where m^*_z is the effective-mass in the z direction. Putting Equation (8) into Equation (1), the L_Q for a planar MOSFET can be obtained as:

$$L_Q = \left| k_B T / (dE_0/dT_{Si}) \right| = \frac{k_B T m_z^* T_{Si}^3}{\hbar^2 \pi^2} \qquad (9)$$

For a SNWT, in general, a 2D Schrödinger equation (in y-z plane) needs to be numerically solved to obtain E_0. It is assumed that the Si body width is always proportional to T_{Si} when calculating L_Q, therefore, E_0 in a SNWT is proportional to $1/T^2_{Si}$ (as in a planar FET), that is:

$$E_0 = \frac{C}{T_{Si}^2} \qquad (10)$$

Where, C is independent to T_{Si} and it can be evaluated after numerically computing E_0.Inserting Equation. (8) into Equation (1), the quantum confinement length L_Q for a SNWT is obtained as:

$$L_Q = \frac{k_B T}{2C} T_{Si}^3 \qquad (11)$$

It is obtained in Equation (9) and (11) that in either a planar or a non-planar FET the quantum confinement length L_Q is proportional to T_{Si}^3, thus, indicating that L_Q is quite sensitive to Si body thickness. So, a trade-off between L_E and L_Q arises. In order to achieve better electrostatic integrity, smaller L_E and smaller body thickness (T_{Si}) is preferred which will, however, cause larger threshold voltage variation.

4. I_{on}/I_{off} for Double Gate MOSFET and SNWT:

To prove above analytical results, a plot in drain current versus gate voltage is simulated using FETToy tool for SNWT and DG-MOSFET and finally ration of I_{on}/I_{off} of both is evaluated to get the result.

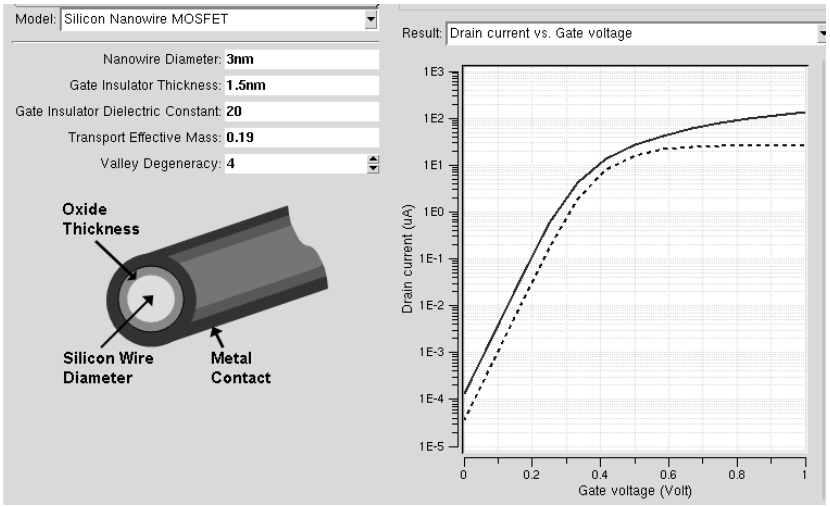

Figure 2: Drain current vs. gate voltage for simulated SNWT

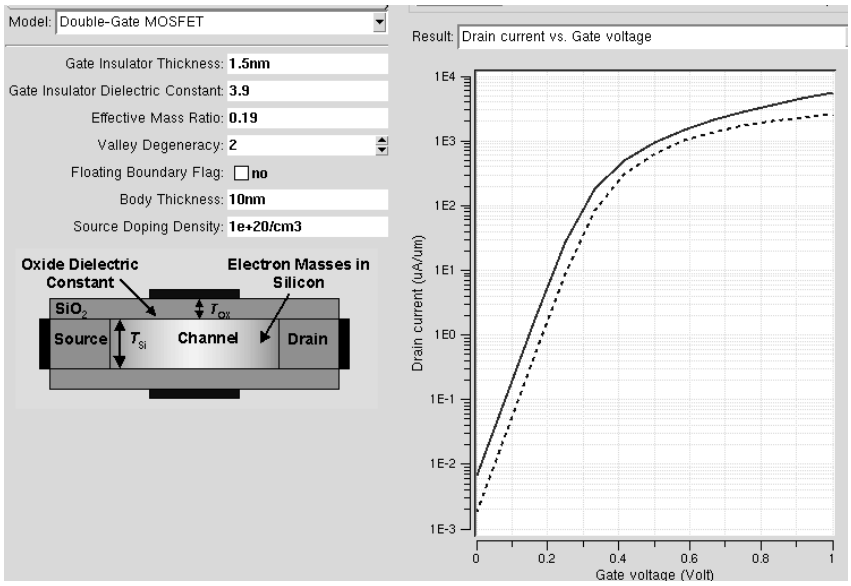

Figure3: Drain current vs. gate voltage for Double gate MOSFET

From figure 2, the I_{on} and I_{off} ratio calculated as:

I_{on} = 134 μA at V_G = 1V

I_{off} = 0.000132 μA at V_G = 0V

Thus, I_{on} / I_{off} = 134 μA / 0.000132 μA = 1.015×10^6

From the figure 3,I_{on} and I_{off} ration for DG-MOSFET is obtained as:
$I_{on} = 5.47 \times 10^3$ μA at V_G=1V
I_{off} = 0.000672 μA at V_G = 0V, thus
$I_{on} / I_{off} = 5.47 \times 10^3$ μA / 0.000672 μA
$= 8.139 \times 10^5$

5. Simulation of DG MOSFET using FETToy (Drain current vs. gate voltage)

Drain voltage = 1.0 (V)

Gate voltage (Volt), Drain current (μA/μm)

0,	0.00672
0.0833333333333,	0.114
0.166666666667,	1.92
0.25,	27.5
0.333333333333,	178
0.416666666667,	493
0.5,	934
0.583333333333,	1480
0.666666666667,	2110
0.75,	2830
0.833333333333,	3640
0.916666666667,	4520
1,	5470

Drain voltage = 0.0833333333333 (V)

Gate voltage (Volt), Drain current (μA/μm)

0,	0.00187
0.0833333333333,	0.0318
0.166666666667,	0.539
0.25,	8.66
0.333333333333,	84.6
0.416666666667,	309
0.5,	638
0.583333333333,	1010
0.666666666667,	1380
0.75,	1730
0.833333333333,	2040
0.916666666667,	2320
1,	2570

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6. CONCLUSION

In this paper, we investigated EQ approach to access the scaling potential of SNWTs vs. planar MOSFETs based on both gate control (electrostatics) and quantum confinement. The result shows that the non-planar nanowire structures, e.g., the cylindrical wire FET, provides better gate control while displaying stronger quantum confinement than planar devices (e.g., double gate MOSFETs). Together, we compared the I_{on} and I_{off} ratio of silicon nanowire transistors and found that Ion and I_{off} ratio of SNWT is greater than the planar MOSFET.

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